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HEWLETT-PACKARD COMPANY
ATTN: Bill Streeter
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

| EXAMINER | |
|---|---|
| MATTHEW, AARON D | |

| ART UNIT | PAPER NUMBER |
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| 2114 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/061,435 | KONDO ET AL. | |
| | Examiner | Art Unit | |
| | Aaron D Matthew | 2114 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18, 22-35, and 38-39* is/are rejected.

7)☒ Claim(s) *19-21,36, 37, and 40-42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-42 have been examined.

### *Claim Objections*

2. Claims 32, 34, 36 and 37 are objected to because of the following informalities:

   - Claim 32 recites "a bridge to an external network" on line 2. This is considered by the examiner to be redundant in view of the amendment made to claim 22, to include the limitation of "a bus bridge to a network". This causes confusion when referring to the bridge to the network in lines 4 and 5 of claim 32, and line 1 of claim 37.
   - Claim 34 has been amended and should be indicated as "currently amended" in the parentheses preceding the claim language.

   Appropriate correction is required.

   Claims 36 and 37 are objected to because of their dependence on claim 32.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 3, 5, 24, and 26, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites the limitation "the expiry of the predetermined time" in line 12. There is insufficient antecedent basis for this limitation in the claim. Applicant indicated, on page 12 of applicant's remarks, that claim 3 had been amended to include the subject matter of claims 1 and 2, however, the subject matter of claim 2, which introduces the limitation of "a predetermined time", was not included in the language of claim 3.

Claim 24 recites the limitation "the expiry of the predetermined time" in line 9. There is insufficient antecedent basis for this limitation in the claim. Applicant indicated, on page 12 of the applicant's remarks, that claim 24 had been amended to include the subject matter of claims 22 and 23, however, the subject matter of claim 23, which introduces the limitation of "a predetermined time", was not included in the language of claim 24.

Claims 5 and 26 are rejected because of their respective dependence on claims 3 and 24.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 5, 11, 15, 16, 22, 24, 26, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro et al, (US 5,748,873), and further in view of Griffin et al, (U.S. 2002/0152418 A1), and Garnett et al, (US 6,587,961).

Regarding claim 1, Ohguro teaches a method of error recovery in a lockstep computer processing system, the system comprising a primary processor and a secondary processor, comprising the steps of:

- Operating the primary and secondary processors in lockstep, (see col. 1, lines 12-18);
- Receiving an error notification resulting from an error in either the primary processor or the secondary processor, (see col. 1, lines 48-50, and col. 2, lines 66-67);

- Determining if the error is a recoverable error, (col. 3, lines 1-2); and
- If the error is a recoverable error, then
    - Saving the state of either the primary or the secondary processor to a memory, (see col. 2, lines 63-66); and
    - Resetting and restarting the primary and secondary processors using the saved state, (note col. 3, lines 1-8, and 29-31).

Ohguro fails to teach that said system also comprises a bus bridge to a network, and that said bus bridge to the network is disabled if the error is a recoverable error or a non-recoverable error. However, Ohguro does teach that said system comprises a bridge to I/O devices, (see col. 5, lines 63-64).

Griffin teaches a fault-tolerant, lockstep system comprising a bus bridge to a network, (note page 7, paragraph 0072, and page 1, paragraph 0006).

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to substitute the bus bridge to a network, taught in Griffin, for the I/O bridge taught in Ohguro, to achieve a method for a fault-tolerant system capable of communicating with a higher availability of resources.

One of ordinary skill in the art would have been motivated to substitute the network bridge of Griffin for the I/O bridge in Ohguro, because, as is explained in Griffin,

paragraph 0072, said network bridge provides connection to a variety of external resources. One of ordinary skill in the art would have clearly recognized that it would be desirable to provide a computer system that communicates with external resources, such as the system of Ohguro, with the potential to communicate with a variety of external resources, in order to improve the availability of essential information and functionality.

Ohguro, in view of Griffin, fails to teach disabling the bus bridge to the network if the error is a recoverable error or a non-recoverable error before data corruption resulting from the error can propagate onto the network. However, Griffin does teach disabling the line of communication with the network, (see par. 0009, wherein disabling the computing elements indirectly disables the line of communication), in order to prevent data corruption from propagating onto the network, (see par. 0002).

Garnett teaches a lockstep computer processing system, (see col. 2, lines 44-49), wherein a bus bridge to a network is disabled in response to detecting an error, (see col. 1, lines 43-50), while the system attempts to recover from the error, (thus, whether the system is recoverable or non-recoverable; see col. 1, lines 51-55). The bus bridge to the network is disabled before data corruption resulting from the error can propagate onto the network, (see col. 1, lines 55-58).

Griffin, Garnett and Ohguro are analogous art because they are from the same field of endeavor, viz., fault-tolerant, lockstep processing systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious, in view of the teachings of Garnett, to combine the step of disabling the bus bridge to a network, taught in Ohguro, in view of Griffin, in response to detecting a recoverable or non-recoverable error.

One of ordinary skill in the art would have been motivated to combine the teachings because the teachings of Garnett meet an explicitly stated need in the field of fault-tolerant, lockstep processing systems connected to an external network. Garnett states, (see col. 1, lines 55-58), that it is desirable to disable a bus bridge to a network in order to prevent far-reaching failures that can result when said systems are connected to a network. Garnett provides a further improvement over Ohguro-Griffin in that it allows the processing sets to continue to function while said bus bridge is disabled, so that they may operate to diagnose and recover from the error, (see col. 1, lines 51-55). Therefore, one of ordinary skill in the art would have been motivated to disable the bus bridge of Ohguro-Griffin, in the event of a recoverable or non-recoverable error, in order to prevent the error from affecting resources external to the fault-tolerant system, while permitting the system to continue to function to attempt recovery from the error.

Claim 22 is also rejected based on the reasoning applied to claim 1.

Claims 3, 5 and 24, 26 are also rejected based on the reasoning applied to claims 1 and 22 respectively, and in light of the 35 U.S.C. 112, second paragraph, rejection made to claims 3, 5, 24 and 26. The limitation, "wherein, if the error notification is received after the expiry of the predetermined time, then treating the error as a non-recoverable error", has not been considered because it has been determined to be indefinite when combined with the other limitations of the claims, as written.

Regarding claim 32, Ohguro fails to teach a computer system, as described in reference to claim 22, which is configured to:

- detect a divergence in the operation of the primary and secondary processors at the bridge to the network; and
- shut off the bridge to the network immediately unless the error has previously been determined to be a recoverable error.

However, Ohguro does teach detecting a divergence in the operation of the primary and secondary processors, (see col. 2, lines 63-66), and resetting the primary and secondary processors if the error causing said divergence is a recoverable error, (see col. 3, lines 1-8). It has also been shown above, in reference to claim 22, that

one of ordinary skill in the art would have considered it obvious, and would have been motivated, to substitute the network bus bridge of Griffin for the I/O bridge in Ohguro.

Griffin teaches detecting a divergence between two lockstep processors at a network bridge, and shutting off the bridge to the network immediately as a result of a non-recoverable error, (see page 1, paragraphs 0006 and 0009).

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the divergence detection of Griffin with the system of Ohguro, in order to achieve a fault-tolerant system that prevents an error from propagating externally in the event of a non-recoverable fault.

One of ordinary skill in the art would have been motivated to combine the teachings because the teachings of Griffin meet an explicitly stated need in the field of fault-tolerant, lockstep processing systems. In paragraph 0002, Griffin shows that it is critical, in fault-tolerant systems connected to a network, to prevent an error from propagating onto the network, and thus extensively effecting resources external to the local system. The system of Ohguro is already capable of detecting a divergence between the operations of two lockstep processors, and resolving the associated error if said error is recoverable. The system of Ohguro fails, however, to explicitly disclose a means of handling a non-recoverable error, and of preventing a

non-recoverable error from affecting external resources. Thus, the divergence checking system of Griffin offers a distinct advantage when combined with the system of Ohguro, by checking for divergence between processors at the network bridge, to indicate the potential for transmitting faulty data, and to allow the network bridge to prevent a non-recoverable fault from reaching beyond the local system. One of ordinary skill in the art would have been clearly motivated to combine the teachings in order to provide a means for handling non-recoverable errors in Ohguro, which ensures that errors do not affect resources external to the local system.

Claim 11 is rejected based on the arguments presented regarding claim 32, as it recites limitations similar to claim 32, except in the context of a method of error recovery.

Regarding claims 15 and 16, it has already been shown in reference to claim 1, that Ohguro, in view of Griffin, teaches a fault-tolerant system comprising a bus bridge to an external network, wherein the processors are reset upon detecting a non-recoverable error. It is also implicit to the teachings that a reset of the processors includes a reset of the system comprising said processors, (note, Ohguro, col. 1, lines 66-67, and col. 2, line 1; note, also, col. 9, lines 55-65 and col. 10, lines 5-20),

in the event of a non-recoverable error. As the I/O bridge is part of the system of Ohguro, Ohguro implicitly teaches resetting the I/O bridge. Since computer processing operations inherently imply high-speed operations, the examiner determines that the teachings of Ohguro, in view of Griffin, comprise a system wherein the bridge is configured to conduct a high-speed reset and restart. Moreover, it is inherent that a custom bus bridge, (as described in Griffin, paragraph 0072), would necessitate a custom high-speed reset and restart procedure.

5. Claims 2, 10, 23 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro, in view of Griffin and Garnett, as applied to claims 1 and 22 above, and further in view of Horst et al, (U.S. 6,233,702 B1).

Regarding claim 23, Ohguro-Griffin-Garnett teaches a system wherein the error handling module is configured to detect a divergence in the operation of the primary and secondary processors, (note col. 2, lines 63-66), and, as has been shown in reference to claim 22, is configured to receive an error notification from either of the processors.

Ohguro-Griffin-Garnett fails to teach a system wherein the error-handling module is further configured to receive a notification of a divergence in the operation of the

primary and secondary processors before receiving the error notification, the error-handling module being further configured to:

- Wait for a predetermined time after receiving the notification of divergence; and
- If the error notification is received before the expiry of the predetermined time and if the error is determined to be a recoverable error, to treat the error as a recoverable error.

However, Ohguro does teach performing a diagnosis program on the processors if a divergence is detected, to determine which processor is at fault, (see col. 1, lines 51-54).

Horst teaches a lockstep processing system, which is configured to receive a notification of a divergence in the operation of the primary and secondary processors before receiving an error notification, (see col. 77, lines 4-9), the error-handling module being further configured to:

- Wait for a predetermined time after receiving the notification of divergence, (col. 77, lines 55-59); and
- If the error notification is received before the expiry of the predetermined time and if the error is determined to be a recoverable error, to treat the error as a recoverable error, (note col. 79, lines 12-25).

Horst, Griffin, Garnett and Ohguro are analogous art because they are from the same field of endeavor, viz., fault-tolerant, lockstep processing systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the divergence handling teaching of Horst, with the divergence handling teaching of Ohguro-Griffin-Garnett, in order to achieve a divergence handling system which is capable of determining the cause of the divergence, utilizing the teachings of Horst, and, resultantly, determine whether an error can be treated as a recoverable error and what recovery operations are necessary to correct the error.

One of ordinary skill in the art would have been motivated to combine the teachings because the teachings of Horst meet an explicitly stated need in the field of fault-tolerant, lockstep processing systems. Horst states that, (see col. 77, lines 10-54), upon detecting a divergence in the operation of two lockstep processors, it is necessary to complete divergence handling in a short time period, in order to avoid transaction timeouts or unsupportable I/O delays. Thus, by providing a time period during which divergence handling must be completed, the teaching of Horst offers a distinct advantage over Ohguro-Griffin-Garnett. Also, Horst states that it is desirable to minimize disruption in the communication of the processing system, by permitting transmissions to continue in the event of a detected divergence, until a determination can be made as to which processor may be at fault. Once said

determination can be made, the teaching of Horst provides for disabling the faulty processor and continuing the transmission of non-faulty data. This provides a distinct advantage over the teaching of Ohguro-Griffin-Garnett, in improving the continuity of transmitted data in the face of a detected divergence. Therefore, one of ordinary skill in the art would have been motivated to utilize the divergence handling teaching of Horst to achieve said clearly recognized improvements in the lockstep processing system of Ohguro-Griffin-Garnett.

Claim 2 is rejected because it recites limitations similar to claim 23, except in the context of a method of error recovery.

Regarding claim 31, Ohguro-Griffin-Garnett, in view of Horst, teaches a system, as described in reference to claim 23, further comprising a main memory, (see Ohguro, col. 2, lines 55-57), the system being configured to detect divergence by:

- Comparing memory commands generated by the primary processor with memory commands generated by the secondary processor, (note col. 15, lines 50-54, and 64-67; and col. 16, lines 1-6) ;
- Executing only the memory commands generated by the primary processor, (note col. 15, lines 64-67, and col. 16, lines 1-2); and

- Signaling a divergence detection if the memory commands issued by the primary processor differ form the memory commands issued by the secondary processor, (see col. 16, lines 4-6).

Claim 10 is rejected because it recites limitations similar to claim 31, except in the context of a method of error recovery.

6. Claims 4 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro, in view of Griffin and Garnett, as applied to claims 1 and 22 above, and further in view of Marshall et al, (U.S. 5,915,082).

Regarding claim 25, Ohguro-Griffin-Garnett fails to teach that non-recoverable error on the secondary processor is treated as a recoverable error. However, Ohguro does teach that the system is capable of continuing system operation in the event of a failure in either processor, (see col. 2, lines 35-40).

Marshall teaches a lockstep processor system in which an error, which would otherwise be determined a non-recoverable error, (see col. 5, lines 28-33), is treated as a recoverable error if the secondary processor determines that it has failed, (note col. 5, lines 35-38, and col. 6, lines 62-63).

Marshall, Griffin, Garnett and Ohguro are analogous art because they are from the same field of endeavor, viz., fault-tolerant lockstep computer systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious, in view of Marshall, to treat a non-recoverable error as a recoverable error in the system of Ohguro-Griffin-Garnett, in the case that said non-recoverable error is detected on the secondary processor.

One of ordinary skill in the art would have been motivated to combine the teachings because Marshall's solution satisfies a clearly recognized need in the art of lockstep computer systems, explicitly stated in Marshall. Marshall states that it is undesirable to stop a system's operation in the event of a non-recoverable error, (see col. 2, lines 31-35), and that high speed recovery is achieved, (note col. 2, line 58), in a system that treats a failure in a secondary processor as a recoverable error, by simply degrading the redundancy of the system. Therefore, one of ordinary skill would have been clearly motivated to combine the teachings as described above, in order to improve the rate of recovery from otherwise non-recoverable errors, supported by the fault-tolerant system of Ohguro-Griffin-Garnett.

Claim 4 is rejected because it recites limitations similar to claim 25, except in the context of a method of error recovery.

7. Claims 6-9 and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro, in view of Griffin and Garnett, as applied to claims 1 and 22 above, and further in view of Downing et al, (U.S. 4,589,090).

Regarding claim 27, Ohguro-Griffin-Garnett fails to teach that a hardware error that results in a loss of a resource that is not being used by the primary processor is treated as a recoverable error. However, Ohguro does teach identifying and treating a hardware error as a recoverable error, (see col. 3, lines 15-19).

Downing teaches a multiprocessor system in which a hardware error that results in a loss of a resource that is not being used by the primary processor is treated as a recoverable error, (see col. 6, lines 60-65).

Downing, Griffin, Garnett and Ohguro are analogous art because they are from the same field of endeavor, viz., fault-tolerant, multiprocessor systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the fault tolerant system of Ohguro-Griffin-Garnett

with the teachings of Downing, in order to achieve a highly reliable, lockstep processor system capable of continued operation while experiencing non-critical hardware component loss.

One of ordinary skill in the art would have been motivated to combine the teachings because the teaching of Downing introduces a distinct advantage in the field of fault tolerance with direct application to the system disclosed in Ohguro-Griffin-Garnett. As shown in Downing, it is desirable in fault-tolerant computing to allow primary system functions to continue operation in the event of a non-critical system component failure, (note col. 7, lines 2-3). Therefore, one of ordinary skill in the art would have been clearly motivated, in view of Downing, (see also, col. 6, lines 66-68, and col. 7, lines 1-2), to treat a hardware error, that results in the loss of non-essential system functions, as a recoverable error in order to allow primary system operations to proceed.

Regarding claim 28, Ohguro-Griffin-Garnett fails to teach that the error notification reports an error occurring in a hardware resource, and includes an identifier that can be used to determine whether the hardware resource is critical or non-critical. However, Ohguro does teach that the error notification does distinguish between correctable and non-correctable faults, (see col. 7, lines 32-42).

Downing teaches a multiprocessor system in which an error notification reports an error occurring in a hardware resource, and includes an identifier that can be used to determine whether the hardware resource is critical or non-critical, (see col. 7, lines 7-10).

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the fault tolerant system of Ohguro-Griffin-Garnett with the teachings of Downing, in order to achieve a highly reliable, lockstep processor system capable of continued operation while experiencing non-critical hardware component loss. It is implicit that such a combination would also comprise Downing's teaching of using an error notification, that reports an error occurring in a hardware resource, including an identifier that can be used to determine whether the hardware resource is critical or non-critical.

One of ordinary skill in the art would have been motivated to combine the teachings because the teaching of Downing introduces a distinct advantage in the field of fault tolerance with direct application to the system disclosed in Ohguro-Griffin-Garnett. As shown in Downing, it is desirable in fault-tolerant computing to allow primary system functions to continue operation in the event of a non-critical system component failure, (note col. 7, lines 2-3). In order to enable a system to continue primary system functions in such an event, it is necessary that the error notification include an identifier that distinguishes between an error in a critical or non-critical

hardware resource. Therefore, in view of Downing, one of ordinary skill in the art would have been motivated to include an error notification that reports an error occurring in a hardware resource, and identifies said error as occurring in either a critical or non-critical hardware resource, in the system disclosed in Ohguro-Griffin-Garnett, in order to enable said system to permit the continuation of primary system functions in the event of a non-essential resource failure.

Regarding claim 29, note Downing, col. 6, lines 66-68 and col. 7 lines 1-2, in which the hardware resource is ignored and effectively disabled.

Regarding claim 30, note col. 11, lines 44-50, in which the system is reset, and note col. 12, lines 19-21, in which the system is further configured to retry the hardware resource after processor restart to determine if the error in the hardware resource can be cured by a processor reset.

Claims 6-9 are rejected because they recite limitations similar to claims 27-30, respectively, except in the context of a method of error recovery.

8. Claims 12, 13, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro, in view of Griffin, Garnett and Horst, as applied to claims 2 and 23 above, and further in view of Hofstee et al, (U.S. 6,751,749 B2).

Regarding claim 33, Ohguro-Griffin-Garnett-Horst, fails to teach a system, as described in reference to claim 23, wherein the error-handling module does divergence detection by comparing unique signatures of processor state received from the primary and secondary processors. Though, as it has been shown, Ohguro-Griffin-Garnett-Horst, does teach comparing the outputs of the two processors to detect a divergence.

Hofstee teaches a fault-tolerant, lockstep processing system, (note col. 2, lines 31-35), in which an error-handling module does divergence detection by comparing unique signatures of processor state received from primary and secondary processors, (see col. 2, lines 47-58).

Hofstee, Ohguro, Griffin, Garnett and Horst are analogous art because they are from the same field of endeavor, viz., fault-tolerant, lockstep processing systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the comparing of signature for divergence detection, as taught in Hofstee, with the teachings of Ohguro-Griffin-Garnett-Horst,

in order to achieve an improved means of detecting divergence in the system of Ohguro-Griffin-Garnett-Horst.

One of ordinary skill in the art would have been motivated to combine the teachings because the teachings of Hofstee meet a need, well known in the art, of providing a faster processing solution in systems, such as the fault-tolerant system of Ohguro-Griffin-Garnett-Horst. Hofstee teaches that it is faster, and therefore advantageous, to check cumulative signatures at intervals rather than to check each individual result, (note col. 2, lines 56-58). One of ordinary skill in the art would have clearly recognized that the divergence checking of Ohguro-Griffin-Garnett-Horst, by checking each output in order to detect a divergence, would be greatly improved by the signature checking teachings of Hofstee. Therefore, one of ordinary skill in the art would have been motivated to combine said teachings, with the system of Ohguro-Griffin-Garnett-Horst, in order to improve the processing speed in said system.

Regarding claim 34, it is inherent, though not explicitly stated, in the description of the signature generating teachings of Hofstee, described in reference to claim 33, that said unique signatures are generated by applying an algorithm to state information for the primary and secondary processors, (see, again, col. 2, lines 47-58)

Claims 12 and 13 are rejected because they recite limitations similar to claims 33 and 34, respectively, except in the context of a method of error recovery.

9. Claims 14 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro, in view of Griffin and Garnett, as applied to claim 22 above, and further in view of Horrigan et al, (U.S. 6,658,532 B1).

Regarding claim 35, Ohguro-Griffin-Garnett teaches that the reset and restart of the primary and secondary processors includes the step of flushing the cache memory of either the primary or the secondary processor, (see, Ohguro, col. 10, lines 12-20)

Ohguro-Griffin-Garnett fails to teach that said step of flushing the cache memory includes conducting first and second flushes of the cache memory.

Horrigan teaches a cache flushing operation comprising a first and second cache flush, (see col. 1, lines 14-17).

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the staged cache flushing operation taught in

Horrigan, with the cache flushing operation taught by Ohguro-Griffin-Garnett, to achieve an improved cache flushing operation during the reset and restart of the primary and secondary processors in the system of Ohguro-Griffin-Garnett.

One of ordinary skill in the art would have been motivated to combine the teachings because the cache flushing operation of Horrigan offers an explicitly stated advantage over the cache flushing operation of Ohguro-Griffin-Garnett. Horrigan states, (note col. 3, lines 1-16), that since interrupts cannot be serviced and a cache cannot be accessed during a cache flush, it is desirable to make the cache flush operation as fast as possible. By flushing the majority of the cache during the first stage, at a less critical time, and making the final flush brief, the flush can be immediately followed by a transition without significantly impacting the total duration between memory or cache accesses. Therefore, one of ordinary skill in the art would have been properly motivated to combine the teachings in order to reduce the time before interrupts and cache accesses are enabled, following a cache flush.

Claim 14 is rejected because it recites limitations similar to claim 35, except in the context of a method of error recovery.

10. Claims 17 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro, in view of Griffin and Garnett, as applied to claims 1 and 22 above, and further in view of Burdett et al, (U.S. 6,327,675 B1).

Regarding claim 38, Ohguro-Griffin-Garnett fails to teach that the system, described in reference to claim 22, further comprises a watchdog timer, the system treating the error as a non-recoverable error if the watchdog timer expires during the reset and restart of the primary and secondary processors. However, Ohguro-Griffin-Garnett does teach some means for determining whether a fault is recoverable, and resetting the primary and secondary processors in the event of a fault, (see col. 3, lines 33-37, and col. 2, lines 60-63).

Burdett teaches a fault-tolerant, multiprocessor system in which an error is detected, and the error is treated as a non-recoverable error if a watchdog timer expires during the reset and restart of the primary processor, (see col. 1, lines 36-48, and col. 2 lines 12-14).

Burdett, Griffin, Garnett and Ohguro are analogous art because they are from the same field of endeavor, viz., fault-tolerant, multiprocessor systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the watchdog timer of Burdett with the fault-tolerant

system of Ohguro-Griffin-Garnett in order to achieve a means of determining whether a fault detected by either the primary or secondary processor is recoverable.

One of ordinary skill in the art would have been motivated to combine the teachings because the watchdog timer taught in Burdett meets an explicitly stated need of Ohguro-Griffin-Garnett. Ohguro-Griffin-Garnett teaches that a fault detected by either the primary or secondary processor should be determined to be recoverable or non-recoverable. Moreover, Ohguro-Griffin-Garnett shows that, in the event of such a fault, the primary and secondary processors are to be reset as a means of attempting to correct the fault. Burdett teaches that when a processor is reset in attempt to correct a fault, a non-recoverable error is indicated when said processor is unable to restart before the expiration of a watchdog timer. By combining the watchdog timer taught in Burdett with the fault-tolerant system taught in Ohguro-Griffin-Garnett, the system of Ohguro-Griffin-Garnett is capable of correcting a recoverable error by a system reset, and indicating a non-recoverable error when such a correction is not possible, thus meeting the need expressed in Ohguro-Griffin-Garnett.

Claim 17 is rejected because it recites limitations similar to claim 38, except in the context of a method of error recovery.

11. Claims 18 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohguro, in view of Griffin, Garnett and Burdett, as applied to claims 17 and 38 above, and further in view of Davis, (U.S. 5,345,583).

Regarding claim 39, Ohguro-Griffin-Garnett-Burdett, fails to teach a system as described in reference to claim 38, wherein the system conducts a hard-reset of the lockstep computer processing system upon expiry of the watchdog timer. However, Ohguro-Griffin-Garnett-Burdett, does teach that the expiry of the watchdog timer indicates that the previous reset was incapable of correcting an error determined to be non-recoverable.

Davis teaches a fault-tolerant system in which a hard-reset is conducted when other resets are incapable of correcting a fault condition, (see col. 5, lines 48-58, and col. 6, lines 15-20).

Davis, Ohguro, Griffin, Garnett and Burdett are analogous art because they are all from the same field of endeavor, viz., fault-tolerant processing systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the teachings of Davis with the fault-tolerant system of Ohguro-Griffin-Garnett-Burdett, in order to achieve an automatic means of

attempting to correct a system error that is otherwise determined to be non-recoverable.

One of ordinary skill in the art would have been motivated to combine the teachings because the hard-reset of Davis meets an implicit need of Ohguro-Griffin-Garnett-Burdett. It would have been clearly recognized by one of ordinary skill in the art, in view of Ohguro-Griffin-Garnett-Burdett, that it is desirable in fault-tolerant systems to quickly and automatically resolve system errors, in order to allow system functions to proceed without human intervention. The system of Ohguro-Griffin-Garnett-Burdett, treats an error as a non-recoverable error in the event that a watchdog timer expires before a faulty processor is capable of restarting. As it is always desirable in fault-tolerant systems to provide an automatic solution to a fault condition, one of ordinary skill in the art would have been clearly motivated to combine the hard-reset taught in Davis, with the system of Ohguro-Griffin-Garnett-Burdett, in order to achieve a means of automatically correcting an otherwise non-recoverable error.

Claim 18 is rejected because it recites limitations similar to claim 39, except in the context of a method of error recovery.

***Allowable Subject Matter***

12. Claims 19, 20, 21, 40, 41 and 42 remain objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, as indicated in the prior office action.

13. Claims 36 and 37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 19, 20, 21, 40, 41 and 42, please see the reasons indicated in the prior office action.

Regarding claims 36 and 37, the limitation, "wherein the bridge is configured to conduct a high-speed reset and restart during the reset and restart of the primary and secondary processors," in combination with the other limitations of the claims, was not found in any prior art.

***Response to Arguments***

15. Examiner notes that claims 3 and 24 were said to have been rewritten in independent form to include all of the limitations of the base claim and any intervening claims. However, as indicated in the rejection made above under 35 U.S.C. 112, second paragraph, the limitations of intervening claims 2 and 23 were not included in the amendments made to claims 3 and 24. Therefore, claims 3 and 24, along with their respective dependent claims 5 and 26, are not believed to be in condition for allowance.

16. Applicant's arguments, see page 11, filed 12/22/2004, with respect to the objection to the drawings, specification and claims, and rejections under 35 U.S.C. 112, have been fully considered and are persuasive. The objections to the drawings, specification and claims, and rejections under 35 U.S.C. 112, made in the prior office action, have been withdrawn.

17. Applicant's arguments, see page 16, filed 12/22/2004, with respect to claims 36 and 37 have been fully considered and are persuasive. The rejection of claims 36 and 37 under 35 U.S.C. 103(a) has been withdrawn. The examiner agrees with applicant that Ohguro does not teach that the reset of the processors includes a reset of the system comprising the processors, in response to a recoverable error. Therefore, the rejection of claims 36 and 37 has been withdrawn, but the rejection of

claims 15 and 16 has not been withdrawn because the language of claims 15 and 16 does not require that the reset and restart of the bridge to the network occur during the restart of the primary and secondary processors. Please note the rejection made above regarding claims 15 and 16.

18. Applicant's arguments, see pages 12-15, filed 12/22/2004, regarding claims 1, 5, 22 and 26 have been fully considered but they are not persuasive.

On pages 13-14, applicant argues that "Griffin does no more in [0072] than teach 'a connector interface (not shown) that facilitates the physical and electrical connection of the server 20 to external resources', exemplifying 'an external interface that provides a connection to an external network via, for example, an RJ-45 connector or coaxial cable connection.' This does not correspond to 'a bus bridge to a network' as recited in claim 1..." The examiner respectfully disagrees.

"An external interface that provides a connection to an external network via an RJ-45 connector or coaxial cable connection" is considered by the examiner to be a bus bridge to a network. Note that "The Authoritative Dictionary of IEEE Standards Terms" defines a bus as "a signal line or a set of lines used by an interface system to connect a number of devices and to transfer data", and defines a bus bridge as "an interconnect between two or more buses that provides signal and protocol translation from one bus to another". In view of these definitions, a coaxial cable

connection is considered to constitute a "bus", and said external interface, a "bus bridge to a network".

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a bus to network bridge exemplified by a PCI to Server Area Network (SAN) I/O bridge) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant argues on pages 14-15, that "the examiner has relied on Griffin by arbitrarily selecting disclosure of the connector interface disclosed in paragraph [0072], has failed to substantiate operable interchangeability as between Ohguro's I/O adapter IOA (Fig. 1) and Griffin's connector interface (e.g. RJ-45 connector or coaxial connection) as disclosed in [0072]," and that, "modification of Ohguro by Griffin as hypothesized by the Examiner would not permit operation of Ohguro in accordance with Ohguro's teaching and would render Ohguro unsatisfactory for its intended purpose." The examiner respectfully disagrees.

Modification of Ohguro by Griffin, to include the network bus bridge taught in Griffin, was made in order to permit access to the variety of external resources taught in

Griffin, to a system utilizing the fault-tolerant methods of Ohguro. Since both references teach fault tolerance computer systems utilizing lockstep processors, one of ordinary skill in the art would have been encouraged to look to a system such as Griffin to provide this functionality in Ohguro. Although Griffin teaches fail-over to a simplex mode, after fault detection, instead of continuing in a duplex mode, there is nothing taught in either Griffin or Ohguro that would preclude using the fail-over methods taught in Ohguro with the lockstep processors of Griffin, which include said bridge to a network. Moreover, note that Ohguro further teaches an embodiment in which the processors fail-over to a simplex mode upon detection of a fault in either processor, (see col. 3, lines 50-67 and col. 4, lines 1-2).

Applicant argues on page 15, regarding claims 5 and 26, that "the examiner contends: 'Ohguro does teach that said system comprises a bridge to I/O devices, (see col. 5, lines 63-64), and that system resources are to be reset upon detection of a recoverable error', but does not indicate where such disclosure is made in Ohguro". The applicant goes on to point out that, "Ohguro teaches that if 'an occurring fault is so light that the data copy can stay in main memory' – recoverable error – '...the processor resetting program shown in Fig. 5 can be executed." This is interpreted by the examiner as disclosing the resetting of system resources upon detection of a recoverable error.

Applicant further argues, regarding claims 5 and 26, that "Griffin does not remedy the deficiencies of Ohguro because, as discussed above, Griffin teaches that in response to any fault detection, both computers receive a STOP command and system operation is continued using only one of the computers, i.e. a simplex mode; no reference to a system reset is seen in Griffin."

The examiner pointed to Ohguro's teaching of resetting certain system resources upon detection of a recoverable error, because resetting inherently comprises the step of stop or disabling said resource so that it can be restarted in its original state. This was done to draw a parallel to Griffin, which teaches disabling the bridge to a network, (see par. 0009, wherein the processors themselves were determined to be part of the bridge to a network, in its broadest interpretation; this ground for rejection was made moot by the amendment to claims 1 and 22, further specifying that the bus bridge to a network is to be disabled). The examiner did not state that Griffin teaches a system reset, nor is this necessary for Ohguro, in combination with Griffin, to meet the limitations of the claims. Again, note that the teaching of Griffin of failing-over to a simplex mode, does not preclude using the fail-over methods taught in Ohguro with the lockstep processors of Griffin, which include disabling said bridge to a network to avoid propagating corrupted data onto the network, and does not eliminate the motivation presented regarding claims 5 and 26 for combining the teachings of Griffin with Ohguro.

19. Applicant's arguments, see pages 16-18, filed 12/22/2004 have been fully considered but they are not persuasive.

Applicant argues on page 16-17, regarding claims 2, 10, 12, 13, 23, 31, 33 and 34, that, "Horst's teaching is inconsistent with that of Ohguro who requires that in response to detection of e.g. an intermittent fault, corrective action results in continuation of operation of both processors in a duplex mode..." and, "modification of Ohguro by Horst, considered in its entirety, would render Ohguro unsatisfactory for its intended purpose." The examiner respectfully disagrees.

Both Ohguro and Horst teach teach fault tolerance computer systems utilizing lockstep processors, wherein errors are detected upon divergence of the outputs of the two processors. Therefore, one of ordinary skill in the art would have been encouraged to look to a system such as Horst to provide divergence detection functionality in Ohguro. Although Horst teaches fail-over to a simplex mode, after fault detection, instead of continuing in a duplex mode, there is nothing taught in either Horst or Ohguro that would preclude using the fail-over methods taught in Ohguro with the lockstep processors of Horst. Moreover, note that Ohguro further teaches an embodiment in which the processors fail-over to a simplex mode upon detection of a fault in either processor, (see col. 3, lines 50-67 and col. 4, lines 1-2).

Applicant argues on page 17, regarding claims 4 and 25, that "the Examiner neglects to recognize that Marshal explicitly teaches in that event, 'the slave processor degrades the system fault detection by simply disabling itself and disabling the lockstep feature on both processors.' This is simply not the operation taught by Ohguro, (e.g. see col. 3, lines 55 to col. 3, line 8) nor that recited in claim 4 or claim 25." The examiner respectfully disagrees.

Marshall teaches the step in which "the slave processor degrades the system fault detection by simply disabling itself and disabling the lockstep feature on both processors," in response to a non-recoverable error, (see col. 5, lines 32-33), detected on the slave processor, (see col. 5, lines 35-36). By degrading the system's fault detection, instead of stopping the system, (which is the master processor's response to a non-recoverable error, see col. 5, lines 30-33), the system is allowed to continue, and thus, recover from the error. Therefore, Marshall is shown to teach a lockstep processor system in which an error, which would otherwise be determined a non-recoverable error, is treated as a recoverable error if the secondary processor determines that it is failed. This is the operation taught in claims 4 and 25, and, to a lesser extent, in Ohguro, which teaches degrading the lockstep feature of the system to recover from an otherwise non-recoverable error, (see col. 3, lines 60-67 and col. 4, lines 1-2), but fails to specify that this occurs only upon failure of a secondary processor.

Applicant argues on page 17, regarding claims 6-9 and 27-30, that "the Examiner admits Ohguro fails to teach the feature recited in claims 6 and 27 but asserts: '...as has been shown, Ohguro does teach identifying and treating a hardware error as a recoverable error.' It is not clear where in the Office Action this disclosure by Ohguro 'has been shown'..." The examiner would like to point to Ohguro, col. 3, lines 15-19, which teaches that the recoverable error disclosed in the discussion pertaining to claims 1 and 22 is a hardware error.

Applicant further argues that the "disclosure by Downing does no more than teach '...if it is a non-critical hardware component,...machine operation can continue either unaffected or only slightly degraded' (col. 6, lines 62-65). It is not seen how this teaching would have been applicable to Ohguro and it is not treatment of a hardware error 'as a recoverable error' (claims 6 and 27) as set forth in the respective claims 1 and 22." The examiner respectfully disagrees.

The limitations of claims 1 and 22, as taught in Ohguro, pertain to a recovering from an error in a way that will allow system functions to continue as before the error occurred. The teachings of Downing show that an error that occurs in a non-critical hardware component, or a component that is currently unused by the primary processor in carrying out its critical functions, can be ignored, and system functions

can continue without reference to the hardware component in question, (see Downing, col. 6, lines 58-67 and col. 7, lines 1-2). Since system functions can continue as before the error occurred, these errors are treated as recoverable errors.

Applicant also argues that the Examiner's reference to Downing at col. 7, lines 32-42...lacks pertinence to recoverable error correction procedure recited in claim 1 or claim 22. This reference was taken out of context. The examiner, in citing col. 7, lines 32-42, was referring to the disclosure of Ohguro rather than Downing, (please see the rejection regarding claim 28, above).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron D Matthew whose telephone number is (571) 272-3662. The examiner can normally be reached on Mon-Fri, from 8:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Aaron D Matthew
Examiner
Art Unit 2114

ADM

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100